DETAILED ACTION

1. Claims 1-11 and 14-22 have been presented for examination.

Claim Interpretation

2. The Examiner interprets the limitation "to produce a simulated processor performance state without causing an actual ACPI processor performance state change" as where the actual internal frequency of the processor has not been changed **(Specification, [0039], the free running clock, 302 of Adachi)** by throttling a clock control signal supplied to the processor **(Specification, [0061], clock throttling controller, 312)**. While the internal state of the processor has not been changed, externally the state of the processor has changed, as the logic establishes the desired (simulated) processor performance state by causing the processor to be throttled **(Specification, [0060])**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims 1-3, 6-11, 14 and 17-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Cooper et al. (U.S. Patent No. 7,082,542) in view of Adachi (U.S. Patent Application Publication 2006/0041766 A1).**

As per claim 1, Cooper is directed to an apparatus for producing a simulated processor performance state in a processor, comprising: a memory to store an address of an ACPI (Advanced Configuration and Power Interface) throttling register in the processor and a set of throttling bit patterns to be selectively written to the ACPI throttling register **(column 3, lines 30-43)**, and a logic to select a bit pattern from the set of throttling bit patterns, and to write the selected bit pattern to the ACPI throttling register **(column 4, lines 15-29)** but fails to explicitly disclose producing a simulated processor performance state without causing an actual processor performance state change. Adachi teaches producing a simulated processor performance state without causing an actual processor performance state change **([0022], Figure 3 and accompanying text)** as the free-running clock generator **302**, the actual performance state of the processor never changes but the but the simulated processor performance state changes due to the throttling of the throttled clock signal, **307**. Cooper and Adachi are analogous art as they are both from the same field of endeavor, thermal management of integrated circuits. It would have been obvious to an ordinary person skilled in the art at the time of the invention to combine the apparatus of Cooper with the clock throttling control of Adachi in order to provide safe thermal throttling **(Adachi, [0018])**.

As per claim 2, the combination of Cooper and Adachi already discloses the apparatus of claim 1, where the memory is to store an address of an ACPI status register from which a value related to throttling established by writing the selected bit pattern to the ACPI throttling register is to be read **(Cooper, column 5, lines 31-47)**.

As per claim 3, the combination of Cooper and Adachi already discloses the apparatus of claim 1, where the memory is operably connected to a Basic Input Output System (BIOS) configured to facilitate controlling one or more processor functions **(Cooper, column 3, lines 24-29)**.

As per claim 6, the combination of Cooper and Adachi already discloses the apparatus of claim 1, where the set of throttling bit patterns facilitates simulating two processor performance states that correspond to a higher performance state and a lower performance state **(Cooper, column 6, lines 50-64)**.

As per claim 7, the combination of Cooper and Adachi already discloses the apparatus of claim 1, where the processor does not have a variable voltage supply **(Cooper, column 3, lines 1-5)**.

As per claim 8, the combination of Cooper and Adachi already discloses the apparatus of claim 1, where the set of throttling bit patterns facilitates simulating two or more processor performance states **(Adachi, Figure 6)**.

As per claim 9, the combination of Cooper and Adachi already discloses the apparatus of claim 8, where the two or more processor performance states include eight processor performance states simulated by throttling the processor 0%, 12.5%, 25%, 37.5%, 50%, 62.5%, 75%, and 87.5% of the time **(Adachi, Figure 6)**.

As per claim 10, the combination of Cooper and Adachi already discloses the apparatus of claim 1, where the ACPI throttling register is configured to cause the processor to be throttled by assorting a signal on a STOPCLK# line connected to the processor **(Cooper, column 4, lines 49-63)**.

As per claim 11, the combination of Cooper and Adachi already discloses the apparatus of claim 7, where the processor does not have a variable frequency clock **(Cooper, column 5, lines 7-23)**.

As per claim 14, Cooper is directed to a method for causing a processor to operate as though an ACPI processor performance state had been established without actually causing an ACPI processor performance state change comprising: receiving a request to establish an actual processor performance state in a processor **(column 5, lines 51-57)**, accessing a data structure to acquire a throttling bit pattern to

write to an ACPI throttling register and an address for the ACPI throttling register **(column 5, lines 58-65)**, and establishing a simulated processor performance state by writing the bit pattern to the ACPI throttling register **(column 6, lines 50-64)** but fails to explicitly disclose producing a simulated processor performance state without causing an actual processor performance state change. Adachi teaches producing a simulated processor performance state without causing an actual processor performance state change **([0022], Figure 3 and accompanying text)** as the free-running clock generator **302**, the actual performance state of the processor never changes but the but the simulated processor performance state changes due to the throttling of the throttled clock signal, **307**. Cooper and Adachi are analogous art as they are both from the same field of endeavor, thermal management of integrated circuits. It would have been obvious to an ordinary person skilled in the art at the time of the invention to combine the method of Cooper with the clock throttling control of Adachi in order to provide safe thermal throttling **(Adachi, [0018])**.

As per claim 17, the combination of Cooper and Adachi already discloses the method of claim 16, where the actual processor performance state corresponds to one of a higher performance state and a lower performance state **(Cooper, column 6, line 65 – column 7, line 5)**.

As per claim 18, the combination of Cooper and Adachi already discloses the method of claim 16, where the actual processor performance state corresponds to one of two or more user defined processor performance states **(Cooper, column 6, line 65 – column 7, line 5)**.

As per claim 19, the combination of Cooper and Adachi already discloses the method of claim 16, where the actual processor performance state corresponds to one of eight processor performance states including a state where the processor is throttled one of 0%, 12.5%, 25%, 37.5%, 50%, 62.5%, 75%, and 87.5% of the time **(Cooper, column 6, line 65 – column 7, line 5)**.

As per claim 20, the combination of Cooper and Adachi already discloses the method of claim 14, where writing the throttling bit pattern to the ACPI throttling register causes a signal to be asserted on a STOPCLK# line into the processor **(Cooper, column 4, lines 49-63)**.

4. Claims 4-5, 15-16, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Cooper (U.S. Patent No. 7,082,542) in view of Adachi (U.S. Patent Application Publication 2006/0041766 A1) in view of Oshins et al. (U.S. Patent No. 6,980,944 B1).**

As per claim 4, the combination of Cooper and Adachi is directed to the apparatus of claim 1, but fails to explicitly disclose the memory storing an ACPI table, the memory being operably connected to a Basic Input Output System (BIOS) configured to facilitate controlling one or more processor functions. Oshins teaches memory storing an ACPI table being operably connected to a BIOS **(column 5, lines 31-35 and lines 39-55)**. It would have been obvious to an ordinary person skilled in the art at the time of the invention to combine the apparatus for producing a simulated processor performance state of Cooper and Adachi with the ACPI table and BIOS connections of Oshins in order to improve hardware and operating system coordination **(Oshins, column 1, lines 14-23)**.

As per claim 5, the combination of Cooper and Adachi is directed to the apparatus of claim 1, but fails to explicitly specify the logic being configured to establish an ACPI table in a Basic Input Output System (BIOS), where to establish the table includes copying one or more values from the memory to the BIOS. Oshins teaches memory storing an ACPI table being in a BIOS **(column 5, lines 31-35 and lines 39-55)**. It would have been obvious to an ordinary person skilled in the art at the time of the invention to combine the apparatus for producing a simulated processor performance state of Cooper and Adachi with the ACPI table and BIOS connections of Oshins in order to improve hardware and operating system coordination **(Oshins, column 1, lines 14-23)**.

As per claim 15, the combination of Cooper and Adachi is directed to the method of claim 14, but fails to explicitly specify including establishing the data structure as an ACPI table m a Basic Input Output System (BIOS) operably connected to the processor. Oshins teaches memory storing an ACPI table being operably connected to a BIOS **(column 5, lines 31-35 and lines 39-55)**. It would have been obvious to an ordinary person skilled in the art at the time of the invention to combine the apparatus for producing a simulated processor performance state of Cooper and Adachi with the ACPI table and BIOS connections of Oshins in order to improve hardware and operating system coordination **(Oshins, column 1, lines 14-23)**.

As per claim 16, the combination of Cooper, Adachi, and Oshins already discloses the method of claim 15, where establishing the data structure includes writing a set of throttling bit patterns to the ACPI table and writing the address of the ACPI throttling register to the ACPI table **(Cooper, column 5, lines 31-47 and Oshins, column 5, lines 31-35)**.

As per claim 22, Cooper is directed to a computer-readable medium storing processor executable instructions that when executed by a processor cause the processor to perform a method, the method comprising: receiving a request to establish an actual processor performance state in the processor, where the actual processor performance state corresponds to one of a higher frequency state and a lower frequency state **(column 5, lines 51-57)**; writing a set of throttling bit patterns to a data structure and writing an address of an ACPI throttling register to a data structure **(column 5, lines 58-65)**; and writing the bit pattern to the ACPI throttling register to cause the actual processor performance state to be simulated without actually causing an ACPI state change **(column 6, lines 50-64)** but fails to explicitly disclose producing a simulated processor performance state without causing an actual processor performance state change. Adachi teaches producing a simulated processor performance state without causing an actual processor performance state change **([0022], Figure 3 and accompanying text)** as the free-running clock generator **302**, the actual performance state of the processor never changes but the but

the simulated processor performance state changes due to the throttling of the throttled clock signal, **307**. Cooper and Adachi are analogous art as they are both from the same field of endeavor, thermal management of integrated circuits. It would have been obvious to an ordinary person skilled in the art at the time of the invention to combine the method of Cooper with the clock throttling control of Adachi in order to provide safe thermal throttling **(Adachi, [0018])**.

However, the combination of Cooper and Adachi fails to explicitly disclose establishing an ACPI table in a Basic Input Output System (BIOS) operably connected to the processor, where establishing the ACPI table includes writing a set of throttling bit patterns to the ACPI table and writing an address of an ACPI throttling register to the ACPI table; accessing the ACPI table to acquire a throttling bit pattern to write to the ACPI throttling register and an address for the ACPI throttling register. Oshins teaches disclose establishing an ACPI table in a Basic Input Output System (BIOS) operably connected to the processor, where establishing the ACPI table includes writing a set of throttling bit patterns to the ACPI table and writing an address of an ACPI throttling register to the ACPI table**(column 5, lines 31-35) and** accessing the ACPI table to acquire a throttling bit pattern to write to the ACPI throttling register and an address for the ACPI throttling register **(column 5, lines 31-35)**. It would have been obvious to an ordinary person skilled in the art at the time of the invention to combine the apparatus for producing a simulated processor performance state of Cooper and Adachi with the ACPI table and BIOS connections of Oshins in order to improve hardware and operating system coordination **(Oshins, column 1, lines 14-23)**.

5. **Claim 21** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Cooper (U.S. Patent No. 7,082,542) in view of Adachi (U.S. Patent Application Publication 2006/0041766 A1) in view of Bhatia et al. (U.S. Patent No. 6,535,798 B1).**

As per claim 21, the combination of Cooper and Adachi is directed to the method of claim 14, but fails to explicitly disclose including: acquiring an address of an ACPI status register configured to report a value related to throttling the processor; reading the value from the ACPI status register, and selectively reporting a success or error condition based on the value. Bhatia teaches acquiring an address of an ACPI status register configured to report a value related to throttling the processor **(column 12, lines 40-43)**; reading the value from the ACPI status register **(column 12, lines 40-43)**, and selectively reporting a success or error condition based on the value **(column 13, lines 8-18)**. It would have been obvious to an ordinary person skilled in the art at the time of the invention to combine the method for causing simulated processor performance states of Cooper and Adachi with the condition reporting of Bhatia in order to determine if additional performance state changes are required **(Bhatia, column 12, lines 29-36)**.

Response to Arguments

6. Applicant's arguments filed 03/11/08 have been fully considered but they are not persuasive.

7. The claim interpretation as noted above stands as the remarks submitted by the Applicant do not render the interpretation consistent. The internal state is mapped to the ACPI state which remains unchanged while the external state is mapped to the state outside of the ACPI state. Additionally, regardless of whether or not the primary reference alone is inconsistent with the claim interpretation, the combination of the references, including Adachi, is consistent with the claim interpretation.

8. In response to Applicant's arguments on page 9, the 35 U.S.C. 112 rejections are withdrawn, as claims 14 and 18-19 are understood to have no actual performance state change at all.

9. In response to applicant's arguments against the references individually on pages 10-13, one cannot show nonobviousness by attacking references individually where the rejections are based on

combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

10. In response to Applicant's argument that there would be no possible motivation to combine Cooper and Adachi, first Examiner notes that it would have been obvious to a skilled artisan from the teachings of both Cooper and Adachi to modify Cooper with Adachi's clock throttling without actual processor state changes so that no actual processor state change is required.

Next, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). As noted above, the combined teachings of the references suggest to an ordinary person skilled in the art that simulating processor performance states without changing actual processor states would be obvious.

Finally, in response to Applicant's allegation that because Cooper "explains why clock throttling is a bad idea" on page 13 of Remarks that there exists no possible motivation to combine Cooper with Adachi which has clock throttling, while Cooper does detail disadvantages to clock throttling in the Background, doing so does not render any possible combination of Cooper and clock throttling unobvious. Adachi is directed towards an improved method of clock throttling and provides motivation for combination of Cooper, to provide safe thermal throttling **([0018])**.

11. In response to the Applicant's remarks on pages 14-16, as the arguments are the same as on page 13, Applicant is directed to the above remarks.

12. In response to Applicant's argument that Oshins does not teach ACPI table in BIOS, the Applicant is directed to **column 5, lines 39-55**.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. The prior art made of record is not relied upon because it is cumulative to the applied rejection. These references include:

1. U.S. Patent No. 5,983,357 issued to Sun on 11/09/99.
2. U.S. Patent No. 6,016,548 issued to Nakamura et al. on 01/18/00.
3. U.S. Patent No. 6,055,643 issued to Chaiken on 04/25/00.
4. U.S. Patent No. 7,089,433 B2 issued to Chaiken et al. on 08/08/06.
5. U.S. Patent No. 6,446,213 B1 issued to Yamaki on 09/03/02.

14. All Claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suzanne Lo whose telephone number is (571)272-5876. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2297. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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